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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/273,560	HASEGAWA, TAKUMI	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Amendment mailed on August 19, 2004. Claims 1-4 of the application were amended. Claims 1-4 of the application are pending. This office action is made non-final in response to the Request for Continued Examination.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-4 are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility.

Claim 1 includes the limitation, "when making a delay analysis of each path of the logic circuit comprising said at least one circuit, a delay time is selected from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the last input terminal to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to

the logical operation information or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the first input terminal to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information".

Specification Fig. 3, Fig. 6 and 7 and description from Page 7, Line 10 to Page 9, Line 7 describe how this limitation is achieved using an AND gate. However, if one were to use an OR gate or an XOR gate, the above limitation is rendered false and inoperative.

The Hasegawa U.S. patent 5,528,511 shows how when an OR gate is used, "a delay time is selected from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the ***first*** input terminal to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the ***last*** input terminal to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information" (CL1, L28-35).

Since, the above limitation in Claim 1 is not true for elements other than an AND gate, the amended Claim 1 is inoperative and are rejected.

Claim 2 includes the limitation, "when making a delay analysis of a logic circuit, a delay time of each path between a plurality of input terminals and a selected output terminal of said at least one circuit is selected from said delay time information, wherein if said selected output

terminal transitions from a low state to a high state said delay time is selected based on the last input terminal of said plurality of input terminals to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to the logical operation information or if said selected output terminal transitions from a high state to a low state said delay time is selected based on the first input terminal of said plurality of input terminals to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information".

Specification Fig. 3, Fig. 6 and 7 and description from Page 7, Line 10 to Page 9, Line 7 describe how this limitation is achieved using an AND gate. However, if one were to use an OR gate or an XOR gate, the above limitation is rendered false and inoperative.

The Hasegawa U.S. patent 5,528,511 shows how when an OR gate is used, "a delay time of each path between a plurality of input terminals and a selected output terminal of said at least one circuit is selected from said delay time information, wherein if said selected output terminal transitions from a low state to a high state said delay time is selected based on the ***first*** input terminal of said plurality of input terminals to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to the logical operation information or if said selected output terminal transitions from a high state to a low state said delay time is selected based on the ***last*** input terminal of said plurality of input terminals to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information" (CL1, L28-35).

Since, the above limitation in Claim 2 is not true for elements other than an AND gate, the amended claim 2 is inoperative and is rejected.

Claim 3 includes the limitation, "if the logic circuit comprises said at least one circuit, selecting the delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the last input terminal to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitions from a high state to a low state said delay time is selected based on the first input terminal to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information".

Specification Fig. 3, Fig. 6 and 7 and description from Page 7, Line 10 to Page 9, Line 7 describe how this limitation is achieved using an AND gate. However, if one were to use an OR gate or an XOR gate, the above limitation is rendered false and inoperative.

The Hasegawa U.S. patent 5,528,511 shows how when an OR gate is used, "selecting the delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the ***First*** input terminal to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitions from a high state to a low state said delay time is selected based on the ***last*** input terminal to transition from a high state to a low

state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information" (CL1, L28-35).

Since, the above limitation in Claim 3 is not true for elements other than an AND gate, the amended Claim 3 is inoperative and are rejected.

Claim 4 includes the limitation, "if a logic circuit comprises said at least one circuit, selecting the delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the last input terminal to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the first input terminal to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information; and a process step of performing a delay calculation using said selected delay time as a propagation delay time of said at least one circuit".

Specification Fig. 3, Fig. 6 and 7 and description from Page 7, Line 10 to Page 9, Line 7 describe how this limitation is achieved using an AND gate. However, if one were to use an OR gate or an XOR gate, the above limitation is rendered false and inoperative.

The Hasegawa U.S. patent 5,528,511 shows how when an OR gate is used, "selecting the delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected

based on the ***first*** input terminal to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the ***last*** input terminal to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information; and a process step of performing a delay calculation using said selected delay time as a propagation delay time of said at least one circuit" (CL1, L28-35).

Since, the above limitation in Claim 4 is not true for elements other than an AND gate, the amended Claim 4 is inoperative and are rejected.

4. Claim 4 is rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

Independent claim 4 recites, "A computer-readable medium having stored thereon a program for executing: a process step comprising ...". The limitations recited in claim contain various process steps, whose programs are stored in a computer-readable medium. The computer-readable medium and the programs are not statutory subject matter. To be statutory, the computer-readable medium should include computer executable instructions which when executed in a computer performs a process comprising the steps included in the limitations.

Claim Interpretations

5. The amended claims are inoperative, except for the AND type of operation. Therefore the art rejections that follow are based on the assumption that the logic operation involved is an AND type of operation.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al. (BL)** (U.S. Patent 5,274,568) in view of **Hasegawa (HAS)** (U.S. Patent 6,041,168) and further in view of **Hasegawa (HS)** (U.S. Patent 5,528,511).

8.1 **BL** teaches method of estimating logic cell delay time. Specifically, as per Claim 1, **BL** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and

comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

BL does not expressly teach that for at least one of the plurality of circuits, the library further comprises logical operation information. **HAS** teaches that for at least one of the plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HAS** that included for at least one of the plurality of circuits, the library further comprising logical operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; and the delay information for the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the

logical operation information for the at least one circuit. **HS** teaches the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; and the delay information for the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** and **HAS** with the system of **HS** that included the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit;

and the delay information for the at least one circuit being based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit. The artisan would have been motivated because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach that when making a delay analysis of each path of the logic circuit comprising the at least one circuit, a delay time is selected from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the last input terminal to transition from a low state to a high state that causes the selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the first input terminal to transition from a high state to a low state that causes the selected output terminal to transition from a high state to a low state according to the logical operation information. **HS** teaches that how when making a delay analysis of each path of the logic circuit comprising the at least one circuit, if an OR gate is used, a delay time is selected from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the ***first*** input terminal to transition from a low state to a high state that causes the selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the ***last*** input terminal to transition from a high state to a low state that causes the selected output terminal to transition from a high state to a low state according to the logical

operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HS** and include an AND gate in the place of an OR gate, so when making a delay analysis of each path of the logic circuit comprising the at least one circuit, a delay time was selected from the delay time information, wherein if a selected output terminal transitioned from a low state to a high state, the delay time was selected based on the last input terminal to transition from a low state to a high state that caused the selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitioned from a high state to a low state, the delay time was selected based on the first input terminal to transition from a high state to a low state that caused the selected output terminal to transition from a high state to a low state according to the logical operation information. The artisan would have been motivated because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

8.2 As per Claim 2, **BL** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and

comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

BL does not expressly teach that for at least one of the plurality of circuits, the library further comprises logical operation information. **HAS** teaches that for at least one of the

plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HAS** that included for at least one of the plurality of circuits, the library further comprising logical operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; and the delay information for the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit. **HS** teaches the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; and the delay information for the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses

the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** and **HAS** with the system of **HS** that included the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; and the delay information for the at least one circuit being based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit. The artisan would have been motivated because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach that when making a delay analysis of a logic circuit, a delay time of each path between a plurality of input terminals and a selected output terminal of the at least one circuit is selected from the delay time information, wherein if the selected output

terminal transitions from a low state to a high state the delay time is selected based on the last input terminal of the plurality of input terminals to transition from a low state to a high state that causes the selected output terminal to transition from a low state to a high state according to the logical operation information or if the selected output terminal transitions from a high state to a low state the delay time is selected based on the first input terminal of the plurality of input terminals to transition from a high state to a low state that causes the selected output terminal to transition from a high state to a low state according to the logical operation information. **HS** teaches that how when making a delay analysis of a logic circuit, if an OR gate is used, a delay time of each path between a plurality of input terminals and a selected output terminal of the at least one circuit is selected from the delay time information, wherein if the selected output terminal transitions from a low state to a high state the delay time is selected based on the ***First*** input terminal of the plurality of input terminals to transition from a low state to a high state that causes the selected output terminal to transition from a low state to a high state according to the logical operation information or if the selected output terminal transitions from a high state to a low state the delay time is selected based on the ***last*** input terminal of the plurality of input terminals to transition from a high state to a low state that causes the selected output terminal to transition from a high state to a low state according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HS** and include an AND gate in the place of an OR gate, so when making a delay analysis of a logic circuit, a delay time of each path

between a plurality of input terminals and a selected output terminal of the at least one circuit was selected from the delay time information, wherein if the selected output terminal transitioned from a low state to a high state the delay time was selected based on the last input terminal of the plurality of input terminals to transition from a low state to a high state that caused the selected output terminal to transition from a low state to a high state according to the logical operation information or if the selected output terminal transitioned from a high state to a low state the delay time was selected based on the first input terminal of the plurality of input terminals to transition from a high state to a low state that caused the selected output terminal to transition from a high state to a low state according to the logical operation information. The artisan would have been motivated because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

8.3 As per Claim 3, **BL** teaches a method for making a delay analysis of a logic circuit (Col 1, Lines 7-13); comprising the steps of:

referencing a delay analysis library for a plurality of circuits (Col 1, Lines 9-13);

the delay analysis library comprising connection information, delay time information (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

BL does not expressly teach the delay analysis library comprising logic operation information. **HAS** teaches library comprising logic operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of

ordinary skill in the art at the time of Applicant's invention to modify the method of **BL** with the method of **HAS** that included the library comprising logic operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of at least one of the plurality of circuits; and the delay information for the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit. **HS** teaches the logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of at least one of the plurality of circuits; and the delay information for the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each

output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** and **HAS** with the system of **HS** that included the logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of at least one of the plurality of circuits; and the delay information for the at least one circuit being based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit. The artisan would have been motivated because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the last input terminal to transition from a low state to a high state that causes the selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the first input terminal to transition from a high state to a low state that causes the selected output terminal to transition from a high state to a low state

according to the logical operation information. **HS** teaches if the logic circuit comprises the at least one circuit, and if an OR gate is used, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the ***first*** input terminal to transition from a low state to a high state that causes the selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the ***last*** input terminal to transition from a high state to a low state that causes the selected output terminal to transition from a high state to a low state according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HS** and include an AND gate in the place of an OR gate, so if the logic circuit comprised the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitioned from a low state to a high state, the delay time was selected based on the last input terminal to transition from a low state to a high state that caused the selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitioned from a high state to a low state the delay time was selected based on the first input terminal to transition from a high state to a low state that causes the selected output terminal to transition from a high state to a low state according to the logical operation information. The artisan would have been motivated

because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

8.4 As per Claim 4, **BL** teaches a computer-readable medium having stored thereon a program for executing a process step (Col 2, Lines 42-50); comprising:

referencing a delay analysis library for a plurality of circuits (Col 1, Lines 9-13);

the delay analysis library comprising connection information, delay time information (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

BL does not expressly teach the delay analysis library comprising logic operation information. **HAS** teaches that the library comprising logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium of **BL** with the computer-readable medium of **HAS** that included the library comprising logical operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of each one of the plurality of circuits; and the delay information for the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the

logical operation information for the at least one circuit. **HS** teaches the logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of each one of the plurality of circuits; and the delay information for the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** and **HAS** with the system of **HS** that included the logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of each one of the plurality of circuits; and the delay

information for the at least one circuit being based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit. The artisan would have been motivated because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the last input terminal to transition from a low state to a high state that causes the selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the first input terminal to transition from a high state to a low state that causes the selected output terminal to transition from a high state to a low state according to the logical operation information. **HS** teaches if the logic circuit comprises the at least one circuit, and if an OR gate is used, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the ***first*** input terminal to transition from a low state to a high state that causes the selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the ***last*** input terminal to transition from a high state to a low state that causes the selected output terminal to transition from a high state to a low state according to the logical operation

information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HS** and include an AND gate in the place of an OR gate, so if the logic circuit comprised the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitioned from a low state to a high state, the delay time was selected based on the last input terminal to transition from a low state to a high state that caused the selected output terminal to transition from a low state to a high state according to the logical operation information or if a selected output terminal transitioned from a high state to a low state the delay time was selected based on the first input terminal to transition from a high state to a low state that causes the selected output terminal to transition from a high state to a low state according to the logical operation information. The artisan would have been motivated because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach a computer-readable medium having stored thereon a program for executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one circuit. **HS** teaches a computer-readable medium having stored thereon a program for executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one circuit (Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of

ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium having stored thereon a program of **BL** with the computer-readable medium having stored thereon a program of **HS** that included executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one circuit, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

Response to Amendments

9. Applicants' amendments, filed on August 19, 2004 have been considered. Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive. New claim rejections have been included in this Office Action under 35 USC 101.

9.1 As per the applicants' argument that "With respect to claim 1, the combination of Blinne et al., Hasegawa `168 and Hasegawa `511 fails to teach or suggest a delay analysis library comprising delay information for a circuit that is based upon the logical state transitions at the input and output terminals of a logical circuit, where the analysis library stores delay time information based on correspondence between the input terminal logical state transitions and the output terminal logical state transitions, and the delay information is selected based upon certain input/output terminal signal transitions; the combination of Blinne et al., Hasegawa `168 and Hasegawa `511 does not use input terminal logical state transitions, output terminal logical state transitions and delay information in the same manner as the present invention... In the three

references, the propagation delay time for a logic circuit is arrived at using maximum delay times, and there is no discussion of using the input signal transitions and the current logical state of the logic circuit as index to a propagation delay time that is representative of how the logic circuit actually operates; in addition, the combination of Blinne et al., Hasegawa `168 and Hasegawa `511 fails to teach or suggest that a delay time is selected from delay time information according to input terminal and output terminal logical state transitions, as recited in claim 1", the examiner respectfully disagrees.

Blinne et al. teaches the delay analysis system having a delay analysis library (Col 1, Lines 9-13), comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Hasegawa '168 teaches that the library further comprises delay information (Col 1, Lines 58-61 and Col 2, Lines 31-35). **Hasegawa** '168 states that high speed delay verification can be achieved by calculating the delay time ... based on information of the circuit model such as logic information, connecting information and delay information.

Hasegawa '511 teaches that delay information for a circuit that is based upon the logical state transitions at the input and output terminals of a logical circuit; delay time information based on correspondence between the input terminal logical state transitions and the output terminal logical state transitions, and the delay information is selected based upon certain input/output terminal signal transitions; **Hasegawa** '511 does use input terminal logical state transitions, output terminal logical state transitions and delay information in the same manner as the present invention; (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42). **Hasegawa** '511 teaches

that the propagation delay time for a logic circuit is arrived at using the input signal transitions and the current logical state of the logic circuit as index to a propagation delay time that is representative of how the logic circuit actually operates; in addition, **Hasegawa** '511 teaches that a delay time is selected from delay time information according to input terminal and output terminal logical state transitions, as recited in claim 1 (Col 2, Lines 30-42; Col 3, Lines 5-26).

9.2 As per the applicants' argument that "Blinne et al. do not teach or suggest determining delay time based on the current logical state of a circuit and how the input signal transitions will affect that logical state; Blinne et al. ignore the logic operation of the analyzed logic circuit by independently recording each of the many inputs of the logic circuit; inputs not being measured are fixed to a predetermined logic level while measuring the delay time of the remaining input; in calculating the maximum delay time for the logic circuit, Blinne et al. uses the delay time of the input with the longest delay time; for example, this delay time is longer than what would be found in normal AND gate operation, because in that case the output falls as soon as the input with the shortest delay time falls", the examiner takes the position that **Hasegawa** '511 teaches determining delay time based on the current logical state of a circuit and how the input signal transitions will affect that logical state, as explained in Paragraph 9.1 above.

9.3 As per the applicants' argument that "Hasegawa '168 does not even teach or suggest signal transitions, but instead adds a series of maximum delay times together to determine a propagation delay", the examiner takes the position that **Hasegawa** '511 teaches determining

delay time based on the current logical state of a circuit and how the input signal transitions will affect that logical state, as explained in Paragraph 9.1 above.

9.4 As per the applicants' argument that "While the circuit modeling technique disclosed by Hasegawa `511 uses rising and falling signals, Hasegawa `511 still rely upon maximum delay times, stored in the arcs between nodes, for propagation delay time calculations; Hasegawa `511 does not teach or suggest determining delay time for each path based on the logical state transitions at the input and output terminals; the Patent Office argues that Hasegawa `511 discloses the rise/fall transitions of the invention recited in claim 1; however, Hasegawa `511 also specifies that certain paths are "invalid" due to their rise/fall characteristics for certain signals, and that no path that contains an "invalid" identifier is used for delay calculations; ... Hasegawa `511 does not teach or suggest determining delay time based on the current logical state of a circuit and the logical state transitions at the input and output terminals; instead, Hasegawa `511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations; unlike the present invention, Hasegawa `511 does not use all the types of logical state transitions present between the input and output terminals of all paths in a logic circuit when selecting a delay time for a particular signal propagation path through the logic circuit; thus, Applicant submits that the Patent Office cannot fulfill the "all limitations" prong of a prima facie case of obviousness with respect to claim 1, as required by In re Vaeck", the examiner respectfully disagrees.

Hasegawa `511 teaches determining delay time for each path based on the logical state transitions at the input and output terminals; determining delay time based on the current logical state of a circuit and the logical state transitions at the input and output terminals; using all the types of logical state transitions present between the input and output terminals of all paths in a logic circuit when selecting a delay time for a particular signal propagation path through the logic circuit; thus (Fig. 3; Col 1, Lines 28-35 Col 2, Lines 30-42; Col 3, Lines 5-26). Therefore, the Examiner takes the position that the "all limitations" prong of a prima facie case of obviousness with respect to claim 1, as required by *In re Vaeck* is fulfilled.

9.5 As per the applicants' argument that "none of the references teach or suggest providing delay information for a circuit that is based upon the type of signal transitions present at the circuit's input and output terminals as represented by stored logical operation information... none of the references teach or suggest that a delay time is selected from delay time information for each circuit path according to the type of logical state transitions present at both the input and output terminals of a circuit, as recited in claim 1; since none of the references teach or suggest these features of claim 1, Applicant submits that one of ordinary skill in the art would not have been motivated to combine the three references; thus, Applicant submits that the Patent Office cannot fulfill the motivation prong of a prima facie case of obviousness with respect to claim 1, as required by In re Dembiczak and In re Zurko", the examiner respectfully disagrees.

The Examiner requests the applicant's attention to the reply presented in Paragraph 9.1 above. The examiner takes the position that the motivation prong of a prima facie case of

obviousness with respect to claim 1, as required by In re Dembiczak and In re Zurko is fulfilled as explained in Paragraph 9.1 above.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043, till October 27, 2004 and 571-272-3717 after October 27, 2004. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704, till October 27, 2004 and 571-272-3716 after October 27, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
September 20, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER